Page 6, Paragraph beginning at Line 11:

B3 Figs. 5A, 5B, 5C, 5D and 5E are plan views showing first embodiments of the present invention.

Page 6, Paragraph beginning at Line 13:

B4 Figs. 6A, 6B, 6C and 6D are plan views showing second embodiments of the present invention.

Page 6, Paragraph beginning at Line 15:

B5 Figs. 7A, 7B, 7C and 7D are plan views showing third embodiments of the present invention.

Page 6, Paragraph beginning at Line 17:

B6 Figs. 8A and 8B are plan views showing fourth embodiments of the present invention.

Page 6, Paragraph beginning at Line 26:

B7 Figs. 1A, 1B and 1C are sectional views of the multi-domain liquid crystal display device of the present invention. Fig. 2 is a plan view showing of the multi-domain liquid crystal display devices of the present invention, and Fig. 3 and Fig. 4 are sectional views showing the view along lines A-A' and B-B' respectively of Fig. 2.

Page 7 and Paragraph beginning at Line 1:

B8 As shown in the figures, the multi-domain liquid crystal display device according to the present invention comprises first and second substrates, a plurality of gate bus lines 1 arranged in a first direction on the first substrate, and a plurality of data bus lines 3 arranged

in a second direction on the first substrate to define a pixel region. A TFT is formed on each pixel region of the first substrate 31 and comprises a gate electrode 11, a gate insulator 35, a semiconductor layer 5, an ohmic contact layer 6, source and drain electrodes 7 and 9, etc. A passivation layer 37 is preferably formed on the whole first substrate 31. A pixel electrode 13 is connected to the drain electrode 9. An electric field inducing window 51 is formed therein for the passivation layer 37.

B8

Page 7 and Paragraph beginning at Line 27:

To manufacture the multi-domain LCD of the present invention, in each pixel region on the first substrate 31, a TFT is formed comprising a gate electrode 11, a gate insulator 35, a semiconductor layer 5, a ohmic contact layer 6 and source and drain electrodes 7 and 9. A plurality of gate bus lines 1 and a plurality of data bus lines 3 are formed to divide the first substrate 31 into a plurality of pixel regions.

B9

Page 8, Paragraph beginning at Line 3:

The gate electrode 11 and the gate bus line 1 are formed by sputtering and patterning a metal such as Al, Mo, Cr, Ta, Al alloy, or an alloy of the combination of these metals, etc. The gate insulator 35 is formed by depositing SiN_x or SiO_x thereon using a Plasma Enhancement Chemical Vapor Deposition (PECVD) method.

B10

Page 8, Paragraph beginning at Line 9:

Subsequently, the semiconductor layer 5 and the ohmic contact layer 6 are formed by depositing by PECVD and patterning amorphous silicon (a-Si) and doped amorphous silicon (n^+ a-Si), respectively. Also, the gate insulator, a-Si and n^+ a-Si can be deposited by PECVD, continuously, and the a-Si and n+ a-Si is patterned to form the gate insulator 35, the

B11

B1 semiconductor layer 5 and the ohmic contact layer 6. Data bus line 3 and source and drain electrodes 7 and 9 are formed by sputtering and patterning a metal such as Al, Mo, Cr, Ta, Al alloy or an alloy of the combination of these metals, etc.

Page 8, Paragraph beginning at Line 19:

B2 The passivation layer 37 is formed with BenzoCycloButene (BCB), acrylic resin, polymide based compound (for example Polyimide, Polyamide, Polyamic acid, etc.), SiN_x or SiO_x on the whole first substrate 31. And the pixel electrode 13 is formed by sputtering and patterning a metal such as indium tin oxide (ITO). The pixel electrode 13 is electrically connected with the source and drain electrode 7 and 9 of the TFT through a contact hole 39.

REMARKS

The Examiner is thanked for the very thorough consideration given the present application. The Examiner's Office Action dated November 6, 2001 has been received and its contents carefully noted.

Minor changes are made to the specification. No new matter has been entered. Claims 1-56 are currently pending in the application. Reexamination and reconsideration of the application is respectfully requested.

The Examiner objected to the drawings because the alignment layers 18 have not been shown in Figure 3 which is a sectional view from Figure 2. Applicants herewith submit a Drawing Change Authorization Request along with a marked up copy of FIG. 3 showing alignment layer 18.